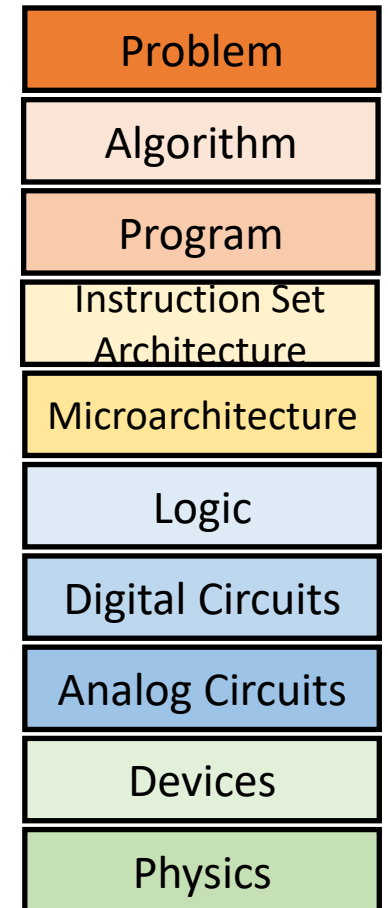


Computer Architecture and Embedded Systems

Prof. Dr. Rolf Drechsler
Dr. Muhammad Hassan
M.Sc. Jan Zielasko
M.Sc. Milan Funck

Winter Semester 24/25



Contact Persons

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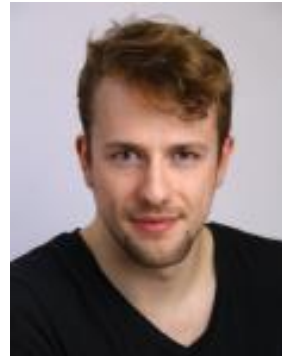
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Organisation

- **Lectures**

- Monday: 14:00 - 16:00, weekly (from 14.10.24)
- Location: MZH 1380/1400
- Language: English

- **Tutorials**

- Tuesday: 08:00 - 10:00, every two weeks or on demand (from 22.10.24)
- Location: MZH 1380/1400
- Language: Deutsch/English

- **Website**

- <http://www.informatik.uni-bremen.de/agra>
 - Lehre -> Lehrmaterial -> Rechnerarchitektur und Eingebettete Systeme 03-IBAP-RA
- Slides and exercises in Stud.IP (<https://elearning.uni-bremen.de/>)

Schedule

Sr.	Lecture	Topics	Tutorials
0	Course organisation	General info	-
1	An Introduction to Computer Architecture	• Important topics in Computer Architectures • From High-level Language to the HW Language • CPU Architecture • Future trends	Designing parts of processor, in particular ALU in Digital (inspired by Logisim).
2	Logic Design – Combinational Circuits	• Truth tables • Boolean algebra • Logic gates • Combinational logic • Hardware description languages	
3	Logic Design – Sequential Circuits	• Clocks • Memory Elements • Finite State Machines	
4	Arithmetic for Computer	• Addition • Multiplication	

Schedule

Sr.	Lecture	Topics	Tutorials
5	RISC-V Assembly Language	Instruction set architecture	• Design and implementation of RISC-V instructions (C++) • Extension of instruction set architecture programming (C++)
6	RISC-V Instruction Format	R, I, S, SB, U, UJ	
7	RISC-V Processor Architecture	• Overview of RISC-V implementation • Building blocks • Implementing add/sub • Implementing ADDI instruction	
8	RISC-V Processor Architecture	• Implementation • Load word • Store word • Branches • Jumps • controller	
9	Pipelining	• Drawbacks of single-cycle processor • Overview of pipelining • Datapath • Control path • Hazards	

Schedule

Sr.	Lecture	Topics	Tutorials
10	From Software to Hardware	• Compiler • Assembler • Linker • Loader • Hello world example	Processor (RISC-V) programming
11	Hardware/Software Co-design - Concepts	• Design methodology • Specification and modelling • characteristics	
12	Hardware/Software Co-design - Synthesis	• System partitioning • Scheduling • Resource sharing	
13	GPU	• Evolution • Design principles • SIMT • SIMD	
14	Future of Computer Architecture	• Challenges • Quantum processors • Neuromorphic processors	

Terms (Scheinbedingungen)

- Technical discussion
 - Successful completion of the exercises required
 - Min. 75% is considered successful per exercise sheet
 - Oral examination, whole group, 20-30 min
 - Includes lecture and exercise
- Module examination
 - Oral exam, individually, 20-30 min
 - Includes lecture and exercise
- Language
 - Deutsch/English
- Fachgespräch
 - Erfolgreiche Bearbeitung der Übungen notwendig
 - Min. 75% Bearbeitung pro Aufgabenzettel
 - Fachgespräch, Gruppenweise, 20-30 min
 - Umfasst Vorlesung und Übung
- Modulprüfung
 - Mündliche Prüfung, einzeln, 20-30 min
 - Umfasst Vorlesung und Übung
- Sprache
 - Deutsch/English

Literature

- D. Patterson, J. Hennessy: Computer Organization and Design RISC-V Edition – The Hardware Software Interface, Elsevier, 2020.
- S. L. Harris, D. Harris: Digital Design and Computer Architecture, RISC-V Edition, Elsevier, 2021.
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- J. Teich, C. Haubelt: Digitale Hardware/Software-Systeme – Synthese und Optimierung, Springer Verlag, 2. Auflage, 2007.
- G. De Micheli: Synthesis and Optimization of Digital Circuits, McGraw-Hill, 1994.
- G. D. Hachtel, F. Somenzi: Logic Synthesis and Verification Algorithms, Kluwer, 1996.

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- H. Kaeslin: Digital Integrated Circuit Design, From VLSI to CMOS Fabrication, Cambridge University Press, 2008.
- A. Biere, D. Kroening, G. Weissenbacher, C. M. Wintersteiger: Digitaltechnik – Eine praxisnahe Einführung, Springer-Verlag, 2008.